Millimeter-Wave Quasi-Optical MEMS Steered MMIC Amplifier Array

Final Report

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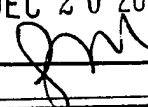
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13. ABSTRACT (Maximum 200 words)

The development of a 44 GHz MEMS-steered solid-state amplifier array with 100 active elements has been studied. The array has a layered geometry with 10 layers of microstrip circuitry, each containing 10 amplifier/MEMS phase shifter elements configured in parallel as a power combining microstrip/parallel plate waveguide combiner. The final strategy for the grating array and layer array amplifiers was implemented and tested. This involved the construction of a compact array amplifier with a beam launcher consisting of an h-plane sectoral horn with an anti-reflection lens. For loss and reflection optimization, several step geometries were studied for the transition to parallel plate. A split transition scheme was introduced for the transition between parallel plate and microstrip. The MEMS phase shifter fabrication process was studied in more detail to expand the total phase shifting range. Severe reliability issues were encountered, especially in terms of DC isolation of the top metal layer. Different techniques have been used to alleviate this problem, which included using different release methods and the use of a wet metal etch. Additionally, a new process for obtaining more compliant MEMS springs without affecting transmission line parameters was successfully developed, therefore allowing actuation of our phase shifters at lower operating voltages.

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1. Foreword

The development of the 44 GHz MEMS steered amplifier array has been carried out through the work of three research teams:

- Raytheon Microelectronics (technical points of contact: Dr. T. Kazior and Dr. N. Kolias): GaAs pHEMT amplifier development, fabrication, characterization, optimization, and packaging integration.

- Cornell SCREAM MEMS Research Group (technical point of contact: Dr. H. Neves): MEMS phase shifter development, fabrication, and characterization.

- Cornell Millimeter Wave Research Group (technical point of contact: Dr. W. Wright): array integration and characterization.

The official start date for the project is June 15, 1997, although the start date for the Raytheon task is October 28, 1997 (date of signature of the Cornell/Raytheon subcontract). A no-cost extension of this contract was granted for an additional year, thus bringing the expiration date to September 30, 2000. Array development work by the Millimeter Wave Research Group was previously supported by ARO funding under Grant DAA H04-94-G-0087.

4.a. Problems Studied

The fabrication process for the MEMS phase shifters was studied in more detail, with vistas to expanding the total phase shifting range by utilizing multiple structures and/or cascading the existing implementation. Severe reliability issues – more specifically regarding the DC isolation of the top metal layer – were encountered and had to be addressed. Different techniques for the final release of the moving structures were investigated to try to alleviate the electric isolation problem. Additionally, a new process for obtaining more compliant MEMS springs without affecting transmission line parameters was developed.

Due to timing issues, a decision was made not to incorporate DBIT to the final architecture. Therefore, Raytheon did not participate in the extended year of this contract.

The final design strategy for the grating array and layer array amplifiers was implemented and tested. This involved the implementation of a compact array amplifier with a beam launcher consisting of an h-plane sectoral horn with an anti-reflection lens. For loss and reflection optimization, several step geometries were studied for the transition to parallel plate. A split transition scheme was introduced for the transition between parallel plate and microstrip.

4.b. Summary of the Most Important Results

4.b.1. MEMS Phase Shifter Work

Metallization Issues

Typical SCREAM (Single Crystal Reactive Ion Etch and Metallization) runs utilize relatively thin metal layers (0.5 μm or less). However, in our case thicker lines were made necessary in order to minimize insertion loss. When thickness is increased, however, the electrical isolation between lines and between a given line and ground starts to fail. We believe that such failure occurs most often at the contact pads where a physical connection between the device and the substrate exists. This was corroborated by verifying that different devices with identical contact pads but different features show similar resistances between the device and the substrate.

One possible way we found for attempting to avoid such a problem was to perform a short wet aluminum etch after the metal deposition step. Although in most cases this actually removes the short circuit, many suspended structures near one another stick together due to capillary forces arisen when drying the device. When two adjacent suspended beams are fully immersed in a liquid, there is no attractive force between them. However, as the beams dry, there comes a point when there is liquid only between the beams. This will exert a capillary pressure between the two beams which is given by [1]

$$q = \frac{2\gamma_l \cos\theta_c}{z}$$

where γ_l is the surface tension of the liquid, z is the space between the two beams, and θ_c is the contact angle (the angle at which the liquid meets the surface). This angle describes the amount of wetting that occurs when the liquid contacts a surface. No wetting occurs when $\theta_c = 180°$, partial wetting occurs when $0° < \theta_c < 180°$, and complete wetting occurs when $\theta_c = 0°$ [2]. Water has a high surface tension and it will, with silicon oxide or metal coating the beams, pull the two beams together. If the beams are compliant enough it will pull them together until they touch. If the material on the beams is fresh (non-passivated), the surfaces will stick together. Of course, the beams will resist the force to some extent depending on how rigid they are in this direction. However, in order to make devices where we can vary the impedances of our lines by large amounts, we want to use beams that are compliant enough that we can perform this impedance-variation with low voltages. This compliance then means the structures will be quite susceptible to these capillary forces. Figure 1.1 shows two adjacent suspended lines before and after an aluminum etch step; the narrow gap between the lines is fused together after this wet processing.
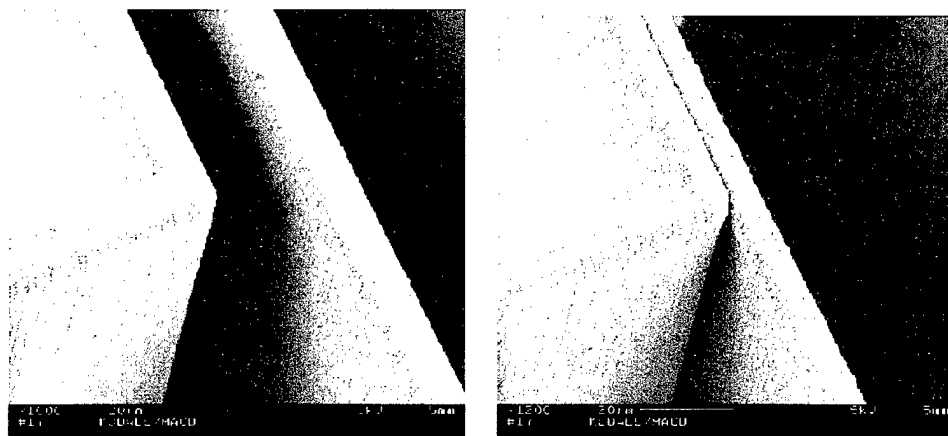
Figure 1.1: SEM micrographs showing two suspended beams before and after wet aluminum etch. Notice that the after the etch the lines are stuck together due to capillary forces.

This problem arises frequently in polysilicon surface micromachining and we have turned to some techniques developed in this area to solve this *stiction* problem. We have used a recipe that passivates the surfaces with a self-assembled monolayer (SAM) coating while they are immersed in the liquid [3]. This consisted of 80 ml of hexadecane, 20 ml of chloroform and 66 drops of OTS. What this coating does is to make the contact angle in the above equation 180 degrees and the capillary pressure negative. When the wafer is removed from the final solution for drying (the final solution being water), the liquid beads up on the surface as does water on a waxed car.

Although this remedy greatly alleviated the electric isolation problem, it was still randomly present to the extent that it was not consistently possible for us to obtain devices which simultaneously presented a low insertion loss and good electric isolation properties.

T-Spring Design

Our MEMS phase shifters have been fabricated using SCREAM, which is a bulk micromachining technique. In bulk micromachining – in contrast with surface micromachining – very high aspect ratios are possible. It is precisely such high aspect ratios that have made feasible the fabrication of our suspended parallel plate transmission lines, ultimately leading to our phase shifters. Additionally, these high aspect ratios are also beneficial in terms of low voltage operation of the electrostatically driven actuators. However, it becomes an obstacle for large displacement operation, given that the suspending springs physically connected to the actuators will also have the same aspect ratio and therefore will be less compliant. Such a trade-off has been resolved in a variety of ways, including a two-depth process, in which all open structures (including springs) will have a shallow depth while closed structures (such as actuators) will be deeper [4]. In our case, however, this technology would deleteriously affect the height of our transmission lines and therefore could not be used. We have therefore devised a new

method for the fabrication of actuators with springs and fingers of different heights that circumvents these problems.

One of the main characteristics of inductively coupled plasma etching is a strong loading effect that causes narrower trenches to etch slower than wider ones. This happens primarily because of the stronger chemical component of the etch when compared to more conventional forms of reactive ion etching. We have utilized this feature to our advantage. We attach silicon beams to both sides of each spring, connecting these beams to the sprigs at a discrete number of points. Figure 1.2 shows a schematic diagram of this strategy. The purpose of these T-shaped structures is to create narrow trenches on both sides of the central spring without adding significantly to the spring constant. The closer the Ts are to a spring, the narrower the trench is and the more difficult it becomes for the chemical etching species (in this case SF_6) to get into and out of the trench. Consequently the central spring will etch more slowly than structures in more open areas such as the fingers of the electrostatic actuators.
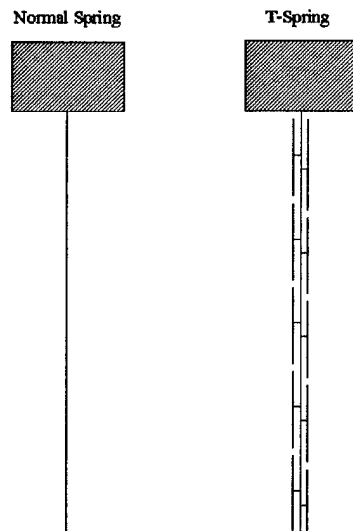

Figure 1.2: Diagram comparing a normal suspended spring with a T-spring, which has T-shaped structures distributed along each side of the spring itself.

This was demonstrated by fabricating two actuators that were identical in every aspect except that one of them had theses Ts incorporated to one of its springs. Figure 1.3 shows SEM micrographs of both devices. Figure 1.4 shows the displacement results at a 25 V bias. A five-fold increase in displacement was observed in the device which contained the Ts. The decrease in the etch rate of the T-spring was confirmed through SEM analysis. Figure 1.5 shows an image of the actuator backbone connected to a T-spring. The first outer T has been broken off to reveal a much shorter spring, which is consequently much more compliant.
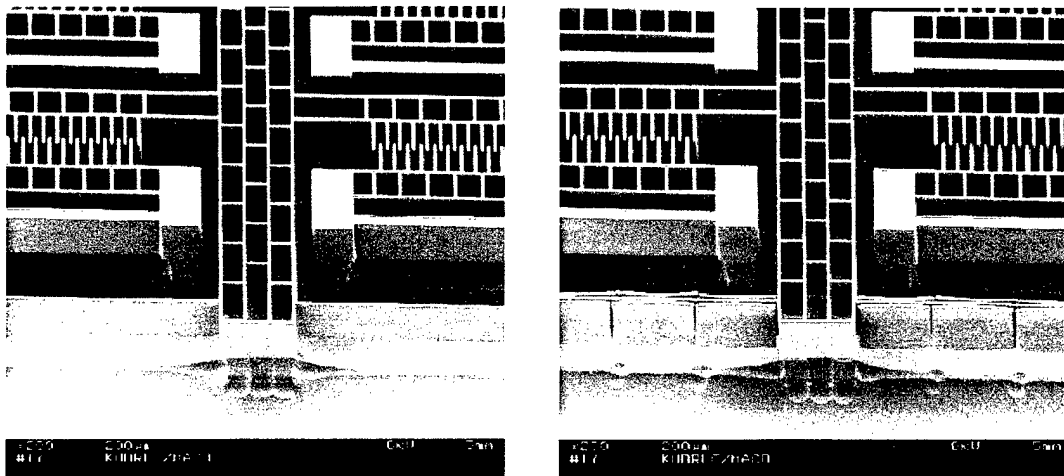
Figure1.3: SEM micrographs showing an actuator suspended with a normal spring (left) and an identical actuator with a T-spring.
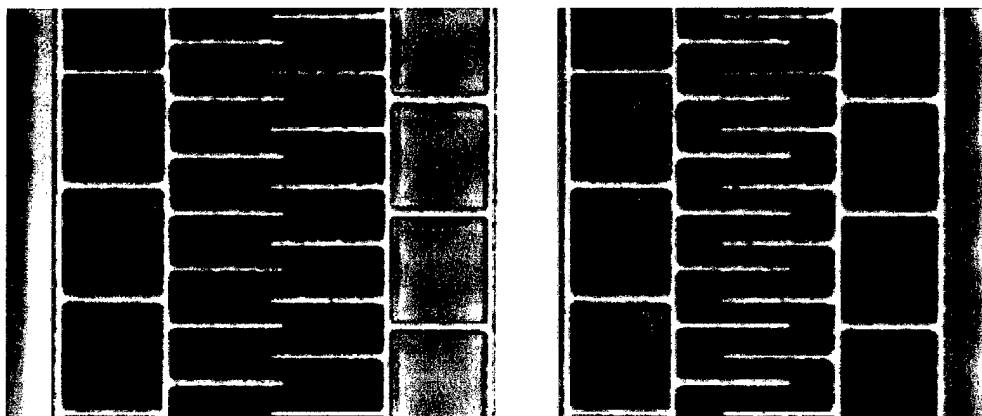

Figure 1.4: SEM micrographs showing a detail of the same actuators shown above when biased at 25 V. The actuator on the left, made with regular springs, presents a displacement of 4 μm at that voltage, whereas the actuator on the right, made with T-springs, has a displacement of 20 μm.
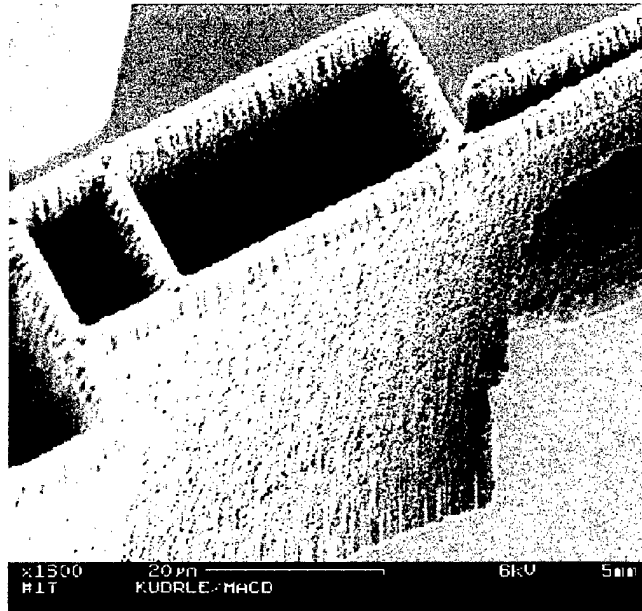
Figure 1.5: SEM micrograph showing the attachment point of a T-spring to the actuator backbone. The first T segment was broken off to show the shallower depth (shown by the arrow) of the central spring.

4.b.2 Array Development

Compact Array Amplifier Design

The compact array design is depicted schematically in Figure 2.1 in its single layer implementation (bottom) and its multi-layer or grating array implementation (top). The view is cross-sectional with propagation from left to right and a vertical E-field. The field is uniform in amplitude in the vertical direction (TEM$_{00}$ propagation) since both top and bottom boundaries are conducting. The entire length is approximately 400 mm for each configuration.
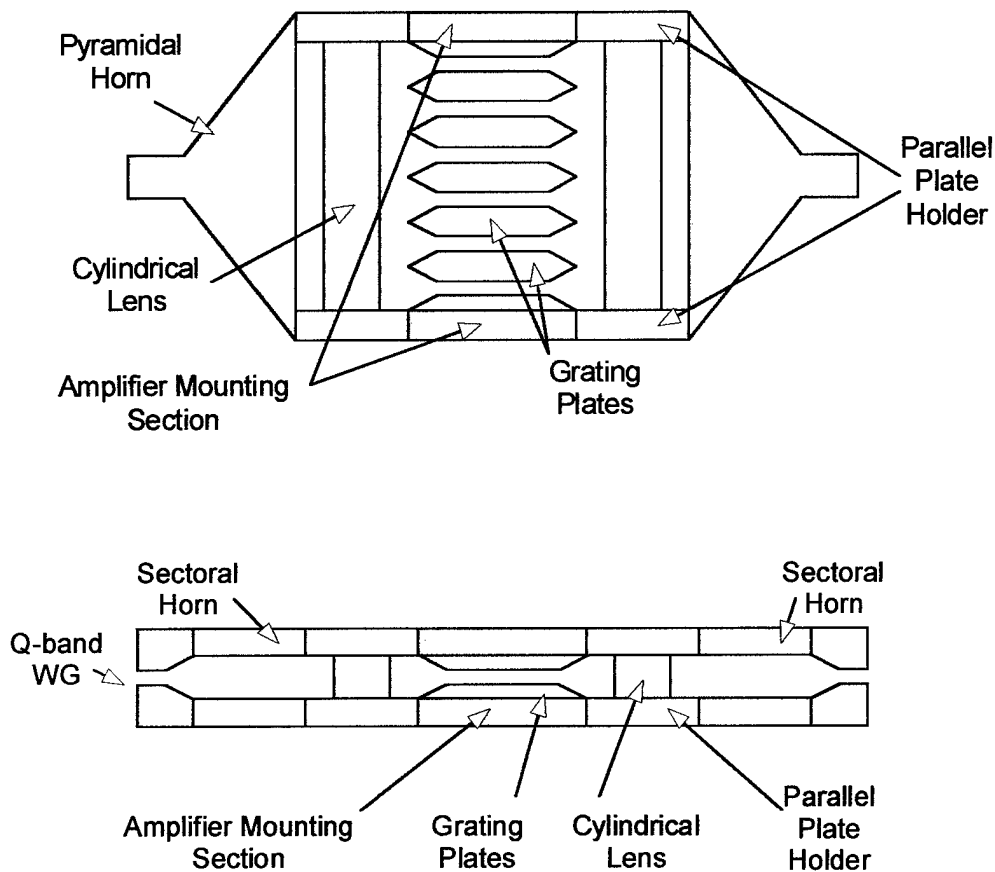

Figure 2.1: The compact array amplifier in its multi-layer array or grating array form (top) and as a single layer array configuration (bottom).

The operation of both configurations is very similar. A detailed account of the experimental implementation is given below following this brief description of operation of the arrays.

For the single layer array a Q-band waveguide input feeds a H-plane sectoral horn antenna to produce a cylindrical wavefront at the horn mouth having a TEM$_{00}$ Gaussian

amplitude profile. This wave propagates through a cylindrical lens to produce a beam with a planar phase front but with a more rectangular amplitude distribution. The lens is designed to redistribute the amplitude profile in this way so as to increase the power combining efficiency of the amplifier from 60% (for a Gaussian beam) to 98% as discussed below and in the 1999 Annual Report. The beam now enters the grating plate region. There is a step height transition to be negotiated from the lens region to the RF circuit board region that is accomplished using a series of quarter-wave parallel plate steps. With this difference the grating plate region is very similar to that of the previous design described in the 1999 Annual Report and has the same two-tier construction for the supply of dc bias to the chips. The beam enters the edge of the RF circuit board – a parallel plate region with an anti-reflection (AR) grooved interface – and is guided into ten individual microstrip circuits using a parallel plate to microstrip transition. Power chips are wire bonded to the microstrip lines and the output from these chips undergoes the inverse propagation path in the output side of the array – microstrip to parallel plate transition, stepped transition, lens, horn to Q-band waveguide output.

For the multi-layer grating array operation is very similar. The input horn is a pyramidal horn in this case so the beam is expanded in the vertical direction but still has a uniform amplitude distribution vertically. The beam propagates through a cylindrical lens with the same shape as the lens in the single layer array to produce a beam a near rectangular amplitude distribution with a planar phase front. The energy in this beam is split into equal portions which enter the separate grating parallel plate regions. There is a stepped transition for the change in vertical step height and now operation in the grating plate array proceeds as per the single layer array. The grating plates with the RF boards and power chips are identical to that used in the single layer array.

The development of the various components of the array is now presented in detail.

H-plane Sectoral and Pyramidal Horns

The H-plane sectoral horns used in the single layer version of the compact array featured Q-band waveguide input and had a 15.5° semi-flare angle and a diameter of 62.0 mm at the horn mouth. The horns had a small flare near the throat to increase the height from Q-band waveguide height of 2.8 mm to 4.25 mm, corresponding to the vertical period of the grating array plate stack. These horns were designed to launch a near Gaussian beam output at the horn mouth with a beam radius of 22.3 mm and phase front curvature of 115.8 mm. Since the horns are to be used while connected to a parallel plate section containing a lens, measurements on the horns were initially made with a parallel plate section attached but containing no lens. (The fields at the horn mouth will be different without the parallel plate section attached.) One-port reflection measurements are shown in Figure 2.2 for Q-band (from 33 to 50 GHz). When absorber is placed over the output face of the parallel plate mouth an improvement in s_{11} of at least 3 dB results so the horn has at least a –20 dB reflection coefficient over the entire Q-band range.

R-Horn No Lens

S11 (db) vs Frequency (GHz)

R-Horn No Lens Abs
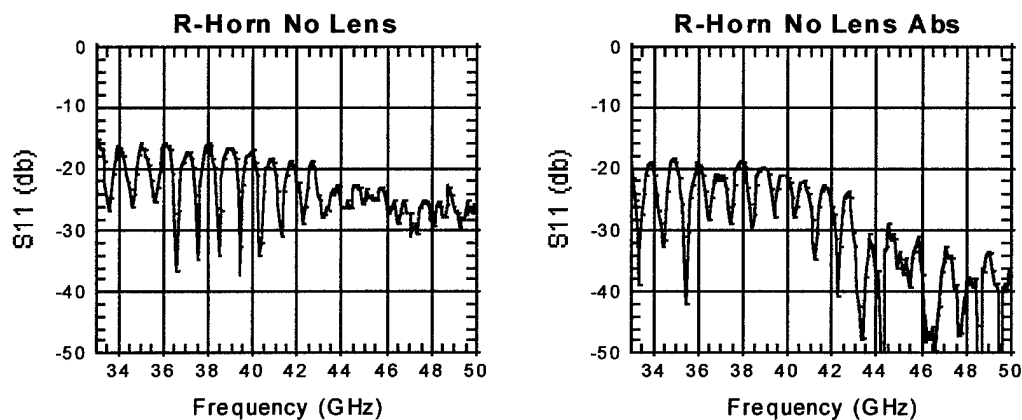
S11 (db) vs Frequency (GHz)

Figure 2.2: One-port reflection coefficients for one of the pyramidal horns with parallel plate output section. *Left:* no absorber over the parallel plate mouth; *Right:* with absorber.
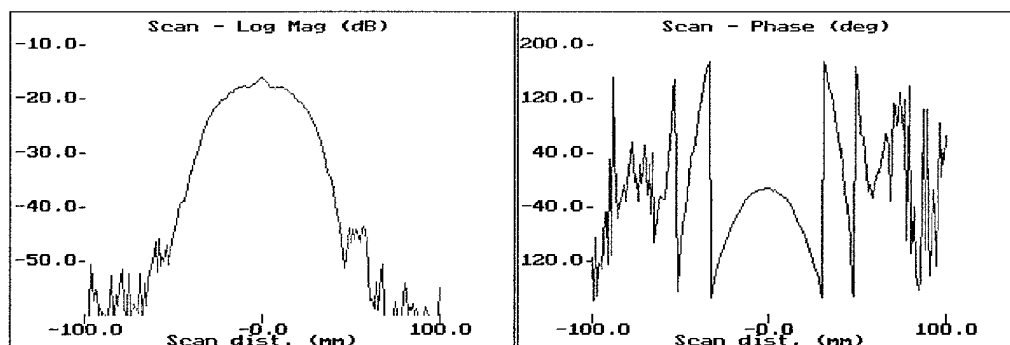

Figure 2.3: Beam scan in the horizontal plane of the output from one of the horns showing field amplitude and phase. The scanning field probe was situated 5 mm from the output face of the launcher.

The output field profile from one of the horns at 44 GHz is shown in Figure 2.3. This is a horizontal scan recorded at a distance of 5 mm from the horn's parallel plate output face. The profile when decomposed into a sum of TEM Gaussian beam modes shows that this profile has a 98% TEM00 content with beam radius 30.4 mm and the phase front radius of curvature 167 mm.

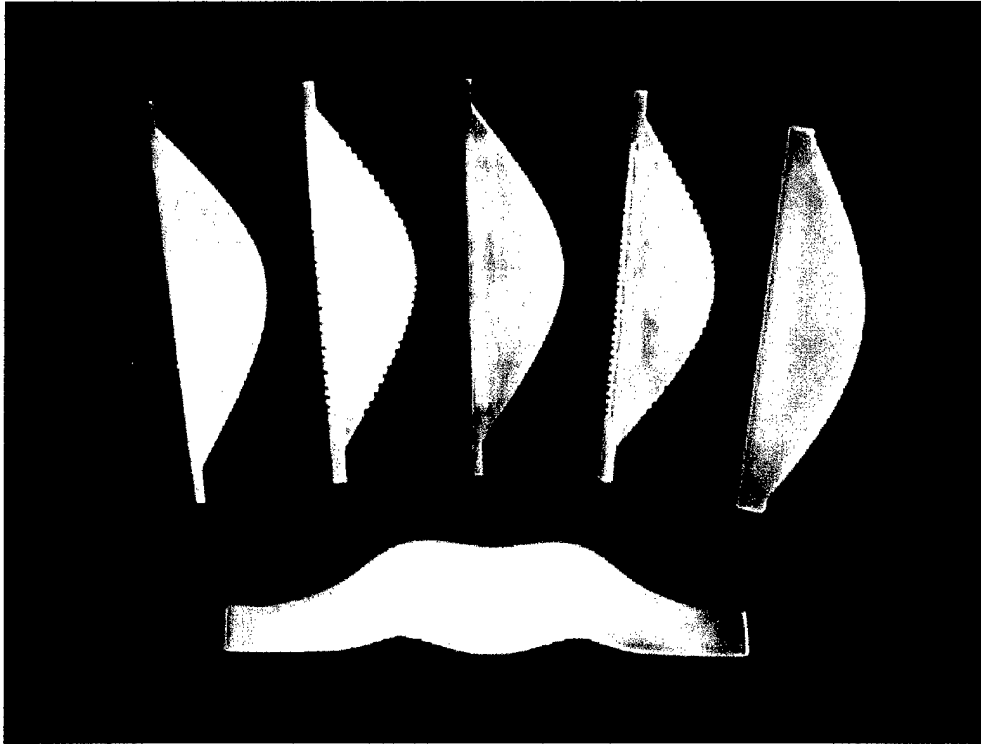# Lens Design and Lens Anti-Reflection Profiling

Figure 2.4: Lenses fabricated for single layer arrays include lenses for Gaussian beam propagation with and without AR profiling (top row) and lenses for redistribution of the amplitude profile (bottom lens).

Rexolite lenses were fabricated in house using numerically controlled milling techniques for the array amplifiers and required anti-reflection surfacing to minimize Fresnel reflections. All the lenses used in the array configurations are cylindrical. For Rexolite the index of refraction is n = 1.594 so that the reflected energy is 5.2% per surface. To reduce this to 1% (-20 dB) per surface, a quarter-wave impedance matching profile was machined into the lens' surfaces. This profile consisted of a series of slots (Figure 2.4) with a regular period small enough to avoid creating diffracted orders and a slot width to ridge width ratio of approximately 2 to 1.

The beam amplitude profile was converted from a Gaussian into a more rectangular shaped profile using a specially designed lens that is shown in Figure 2.4, bottom lens. The design procedure used was a geometrical optics approach, based on the procedure in [5] but modified since the amplitude profile in our geometry is essentially one-dimensional (cylindrical lens design) rather than two-dimensional for a concentric lens. The amplitude profile used in the design is denoted as a $\cos^8$ edge taper in the radio-astronomical literature and has an E-field profile given by:

$$E(x) = 1 - \sin^8(x/a)$$

where the constant, a, characterizes the width of the beam.

The performance of the amplitude-tapered lenses was also compared with that of conventional PCX lenses of comparable focal length. Lenses with and without anti-reflection (AR) surfaces were also compared. These measurements were performed as one-ports using single launcher consisting of a horn with a lens mounted between attached parallel plates, or as two-ports using two launchers connected back-to-back.

Launcher Performance

The H-plane sectoral horn with an AR lens attached in its parallel plate mounting constitutes a beam launcher. The one port reflection coefficients for the input and output launchers, fitted with conventional PCX lenses, and where the reference plane is the Q-band waveguide input, is shown in Figure 2.5.
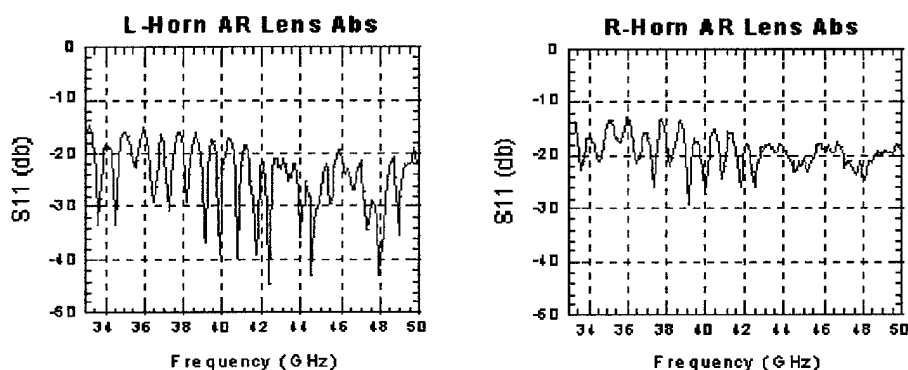
Figure 2.5: Launcher one-port reflection coefficients for the input (left) and output launchers (right) when absorber has been placed over the launcher output face. PCX lenses were installed in both launchers.

These results show a launcher input reflection coefficient approaching the –20 dB level over the upper half of Q-band. The difference in the results above for these two nominally identical launchers is due to the small amount of reflection from the absorber covering the launcher output aperture. Similar results were obtained for the launchers when amplitude tapered lenses were installed in place of PCX lenses. These results are shown in Figure 2.6. The improved performance is believed to be due to the fact that a smaller period was used for the AR slot profile for the amplitude-tapered lenses.
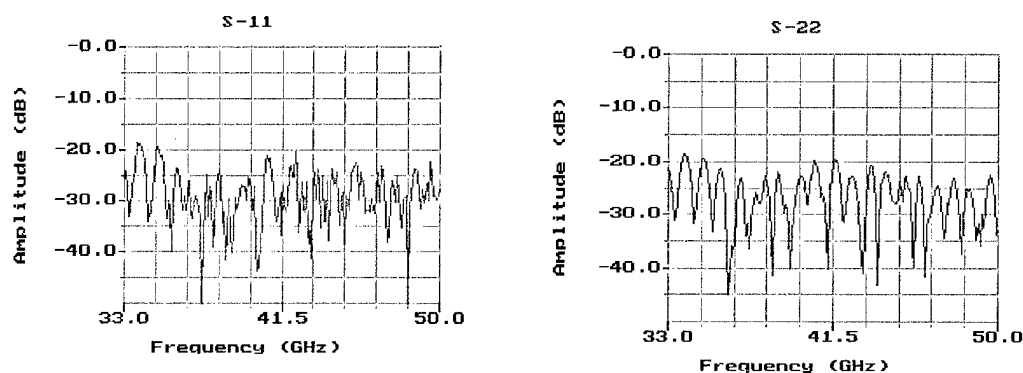
Figure 2.6: Launcher one-port reflection coefficients for the input (left) and output launchers (right) when absorber has been placed over the launcher output face. Amplitude tapered lenses were installed in both launchers.

Beam scans of the radiated E-fields were obtained to ascertain the success of the amplitude tapered lens design. The results in Figure 2.7 show the amplitude and phase for one of the launchers fitted with an amplitude-tapered lens where the beam has been scanned at a distance of 5 mm from the launcher output face. There are 3 curves fitted to the amplitude data (shown separately for clarity), for cos^4 (top left), cos^8 (top right), and Gaussian (bottom left) profiles. The jaggedness evident in the center of the profile is believed to be due to small reflections from the probe waveguide used to sample the E-field. Apart from this the beam profile shows marked 'squaring up' of the amplitude distribution with virtually no residual lobe structure in the wings. The phase, Figure 2.7, bottom right, is flat to within 10° over most of the profile. The beam diameter is 3.5 mm smaller than the design specification of 35.0 mm. Nevertheless, this is a gratifying result given the lens design procedure used a geometrical optics approach.

Using two launchers connected back-to-back we can obtain an idea of the throughput of the basic system as shown in Fig.1 (bottom) but with the amplifier mounting section and grating plates removed. These measurements are shown in Figure 2.8 and represent a 2-port measurement with reference planes at the Q-band waveguide input and output ports.

Intensity – cos^4 fit
Intensity – cos^8 fit
Intensity – gaussian fit
Phase (deg)

Scan dist. (mm)

Data: may2\larcos6
a1: 0.965 a2: -0.914 a3: 32.33   a1: 0.912 a2: -0.753 a3: 27.12
a1: 1.064 a2: -1.165 a3: 18.00
Fitted Parameters:- a1=max. intensity, a2=offset, a3=beam radius.
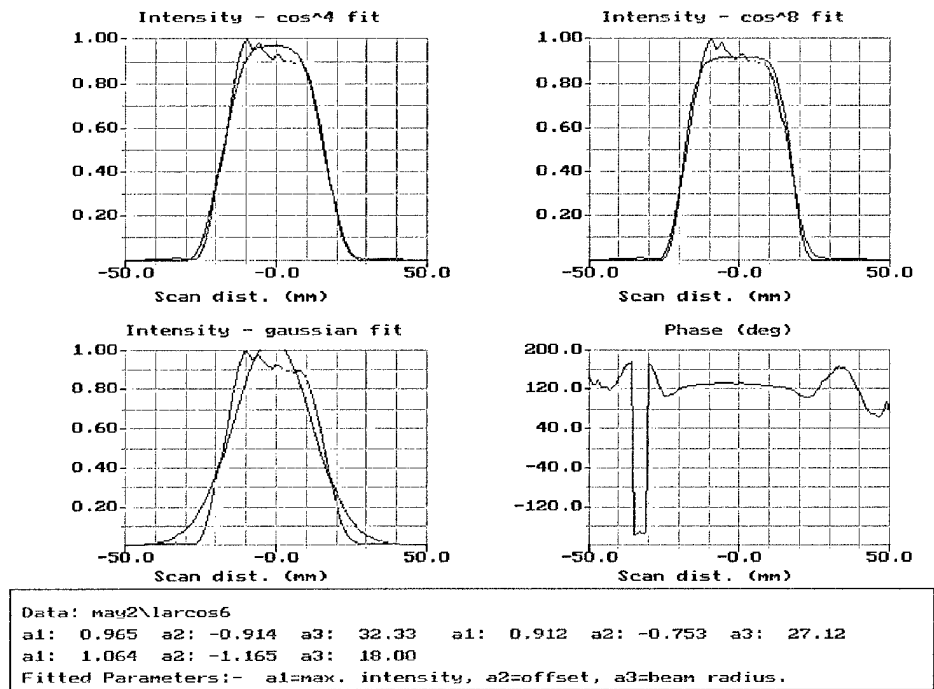
Figure 2.7: Output E-field beam scan for a launcher fitted with an amplitude-tapered lens. The amplitude data is repeated 3 times with different fitted curves.
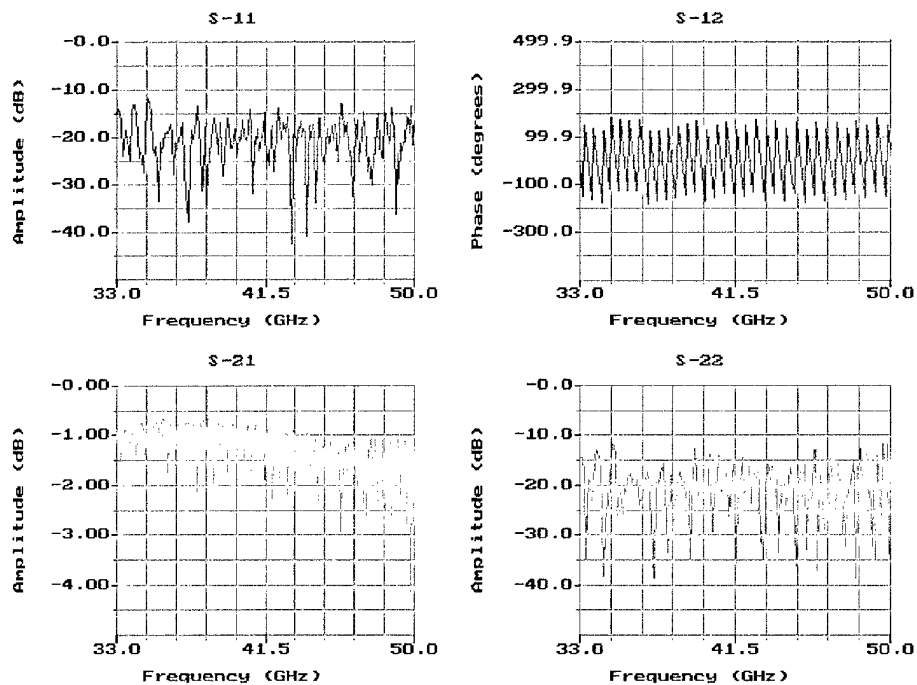

S-11
S-12
S-21
S-22

Amplitude (dB)
Phase (degrees)
Frequency (GHz)

Figure 2.8: S-parameters for two launchers, fitted with amplitude-tapered lenses, and mounted back-to-back.

These results were subsequently marginally improved by adjusting the launchers mechanically. Note that with the launchers joined back-to-back there will be a phase front curvature mismatch since the system was designed with the amplifier mounting section included. A comprehensive loss budget was also performed taking into account all conductive and dielectric losses in the launchers. The loss per launcher was established to be 0.5 dB with an error of ±0.1 dB.

Amplifier Mounting Section

The amplifier mounting section is the heart of this array architecture. For the single layer configuration this consists of one pair of stepped or tapered plates between which is sandwiched a PCB containing the parallel plate to microstrip transitions (Figure 2.1, bottom). For the full grating array there is a stack of such plates and PCBs (Figure 2.1, top).

Stepped Plate Transitions

Several step geometries were designed, modeled, fabricated and tested with the purpose of obtaining a low loss, low reflection transition from the launcher output into the parallel plate region of the PCB. These structures were designed using transmission line theory for quarter-wave stepped impedances and are essentially Butterworth or Chebyshev filter designs.
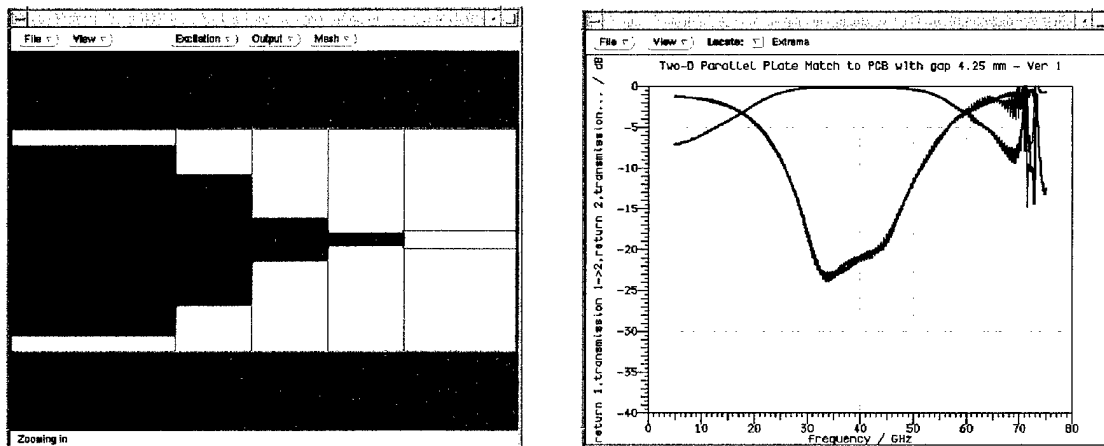

Figure 2.9: Stepped transition matching to the PCB dielectric. *Left:* transition geometry. *Right:* all 4 S-parameters from the MicroStripes simulation. s_{11} and s_{22} overlap and reach –20 dB over Q-band.

A novel approach is the three-step quarter-wave transition matching directly to the PCB dielectric shown in cross-section in Figure 2.9, left. The beam propagates from left to right between air-filled parallel plate steps before entering the 15-mil thick TMM3 dielectric (green slab on the right in Figure 2.9). The design was modeled using a 3-D electromagnetic simulator, MicroStripes, with dielectric and conductive losses included, with the results shown in Figure 2.9, right. Measurements performed on this transition showed, after careful loss budget analysis, an unaccountable loss of 0.8 dB. This could be due to propagation of energy in the tiny gap between the PCB copper cladding and the aluminum mounting plate clamping the PCB or in the gap between the end of the dielectric and the plates but could not be eliminated.

The solution was to move the TMM3 PCB away from the transition steps and cut an AR profile into the edge of the PCB in a similar manner to the AR profile of the lenses. This approach worked satisfactorily and consistently. The disadvantage is that the last step change in height is very small, 33 μm, and careful machining techniques are required. To characterize the stepped plate transitions we connected launchers to a pair of stepped transition plates without a PCB (0.415 mm air gap) and measured the S-parameters referenced to the waveguide input and output ports. The results are shown in Figure 2.10.
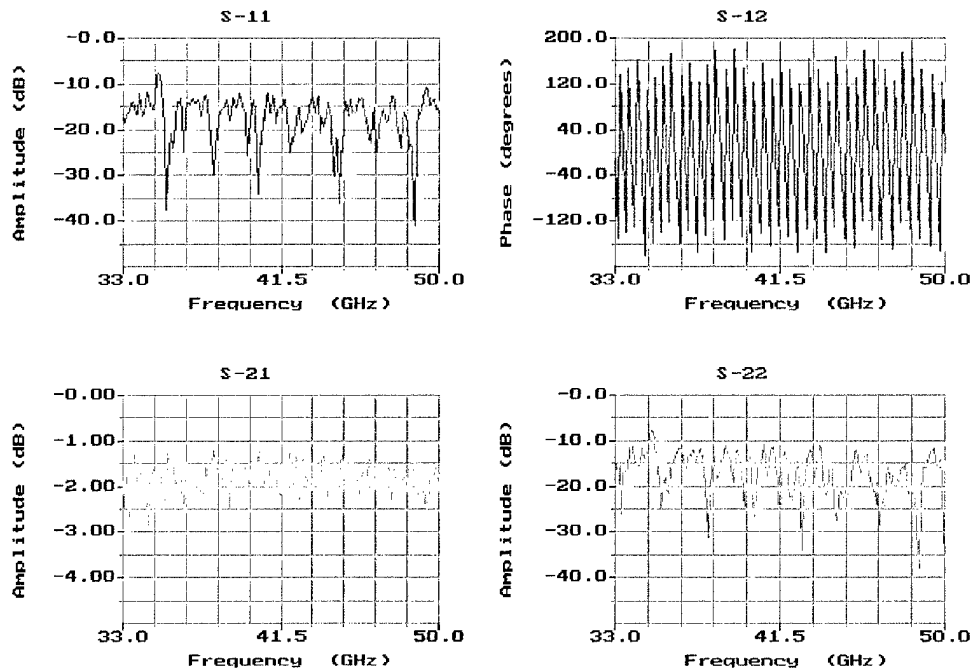

Figure 2.10: Stepped transition S-parameters obtained without a PCB installed between the stepped plates (0.415 mm air gap between plates).

A loss budget for the system gave an insertion loss of 1.43 dB at 44 GHz which compares reasonably well with the measured loss of 1.75 dB.

Parallel Plate to Microstrip PCB Transition

A passive parallel plate to microstrip PCB transition (AUTOCAD drawing) is shown in Figure 2.11. These transitions were fabricated on 15 mil thick TMM3 using a Protomat C60 circuit board milling machine. This machine was used to define the copper circuitry as well as to create the AR profiled edges of the boards.
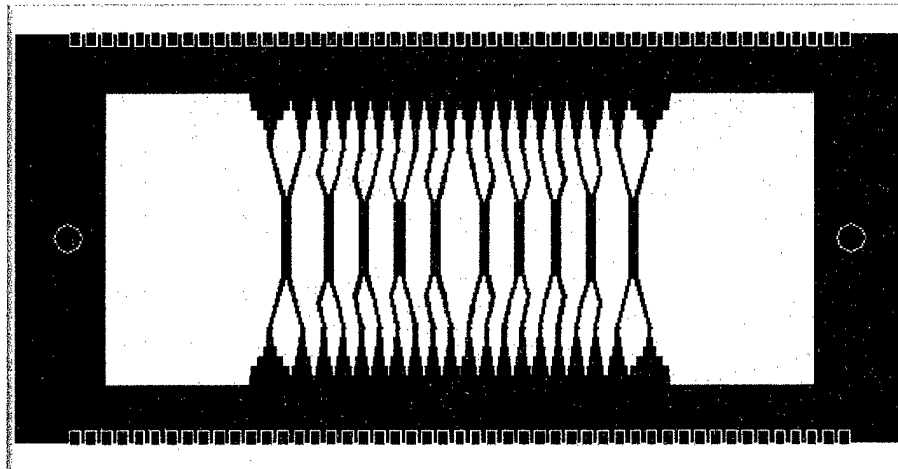

Figure 2.11: AUTOCAD drawing of a passive parallel plate to microstrip PCB for the system using amplitude tapered beam profiles.

The transition consists of a parallel plate section that splits into 20 stepped sections that taper down to 100Ω lines, then pair off to 10 microstrip 50Ω lines. These microstrip lines then flare via an identical set of stepped transitions and dividers to merge again into a single parallel plate waveguide. The stepped sections on the far left and right are wider than the center sections in order to capture the more tapered beam edge. The result is that each microstrip line receives equal energy power from the incident beam. We use 20 stepped transitions combined in pairs, rather than 10 transitions, in order keep all the stepped transition widths below the diffraction limit width of one guide wavelength.

The transition was designed as a collection of coupled microstrip lines where it should be noted that we are only interested in the 'even' mode, i.e. the mode with equal in phase energy on each line. Since there are no formulae in the literature for the synthesis of asymmetrical coupled lines, we heuristically derived such formulae from the symmetrical results and simulated the complete structure using MicroStripes. The final design achieved a reflection coefficient for each stepped transition of better than –18 dB over the entire Q-band with the exception of the end-most cells where the reflection coefficient rose to –13 dB at 40 GHz. Some of these results are shown in Figure 2.12.
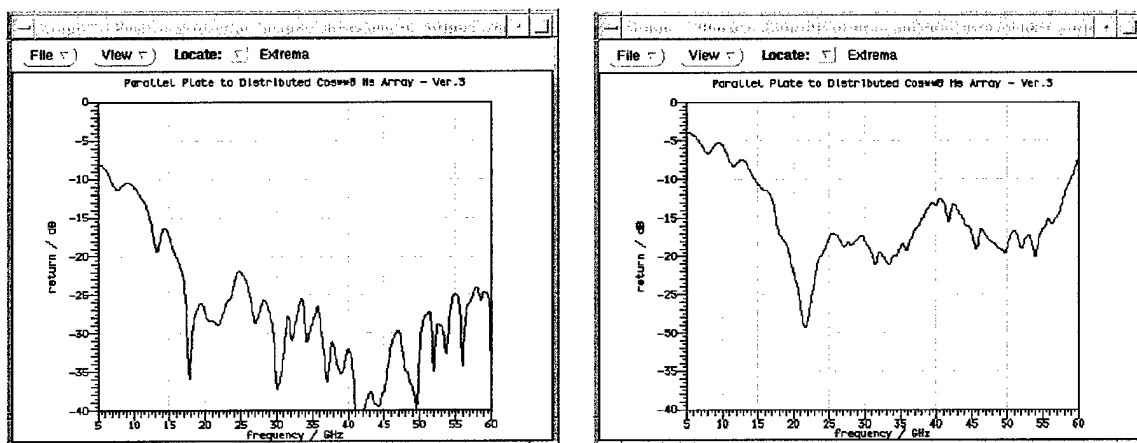
Figure 2.12: Microstripes simulation results showing the reflection coefficient for the inner-most (left) and outer-most (right) stepped transitions of the parallel plate to microstrip PCB transition.
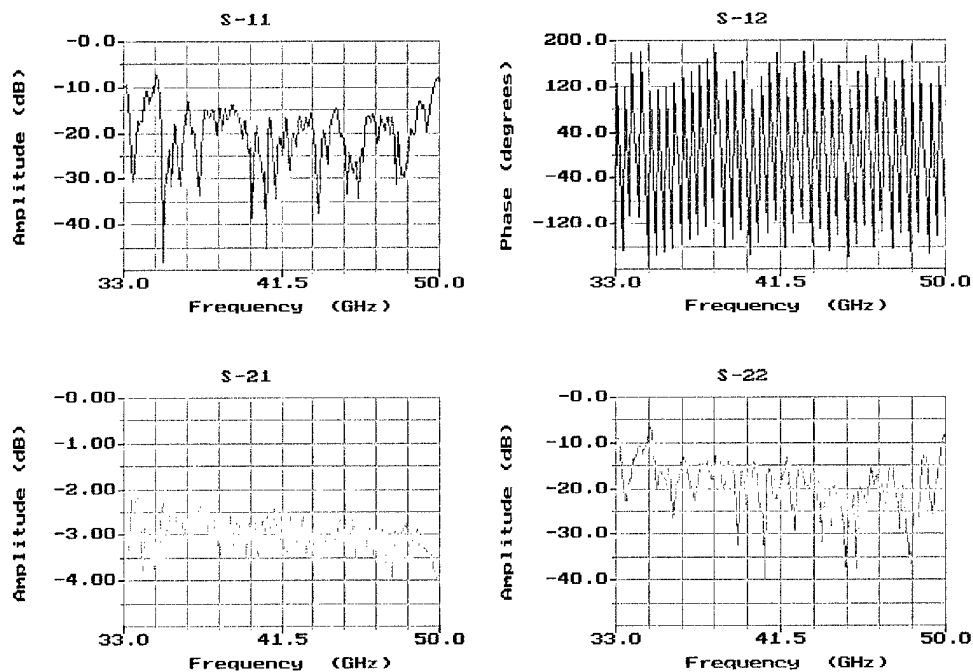

Figure 2.13: Single layer system s-parameters for an AR interfaced parallel plate to microstrip $\cos^8$ cell distribution board.

We are now in position to perform measurements on a passive version of the single layer array depicted in Fig. 1, bottom. The s-parameters for the single layer system using this board are shown in Fig. 14. The insertion loss from waveguide input to waveguide output is approximately 3 dB over Q-band. The theoretical loss budget gives 2.11 dB at 44 GHz. The discrepancy is attributed to the mechanical imperfection of the PCB and the milling process used to create boards with such fine features. Nevertheless, the results are extremely encouraging for a 10-way quasi-optical power combiner.

Single Layer Array Amplifier

Several single layer array amplifiers were constructed using the amplitude tapered beam profile design. The PCB is essentially the same as used in the passive version of the array. Figures 2.14 and 2.15 show such an amplifier under construction and in finished form respectively.
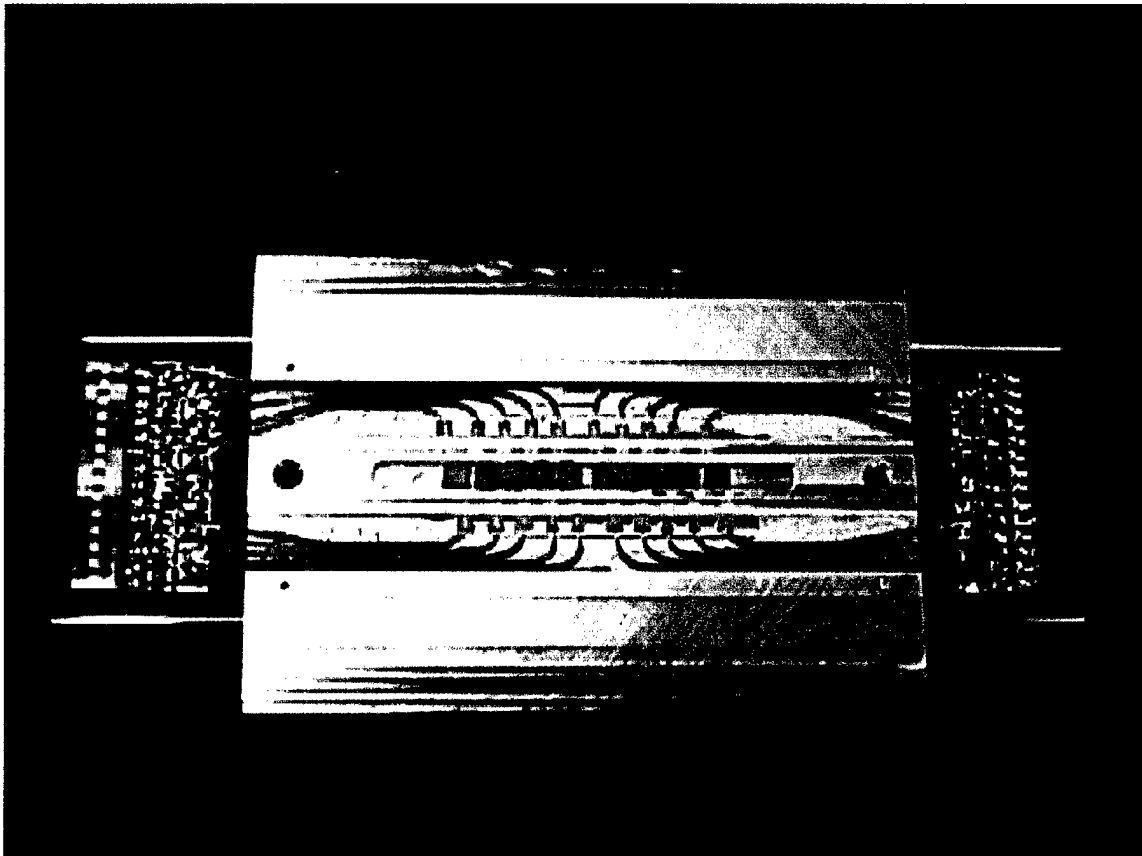

Figure 2.14: Single layer array amplifier before the RF boards and MMICs are installed showing the underlying gate and drain bias supply circuitry.
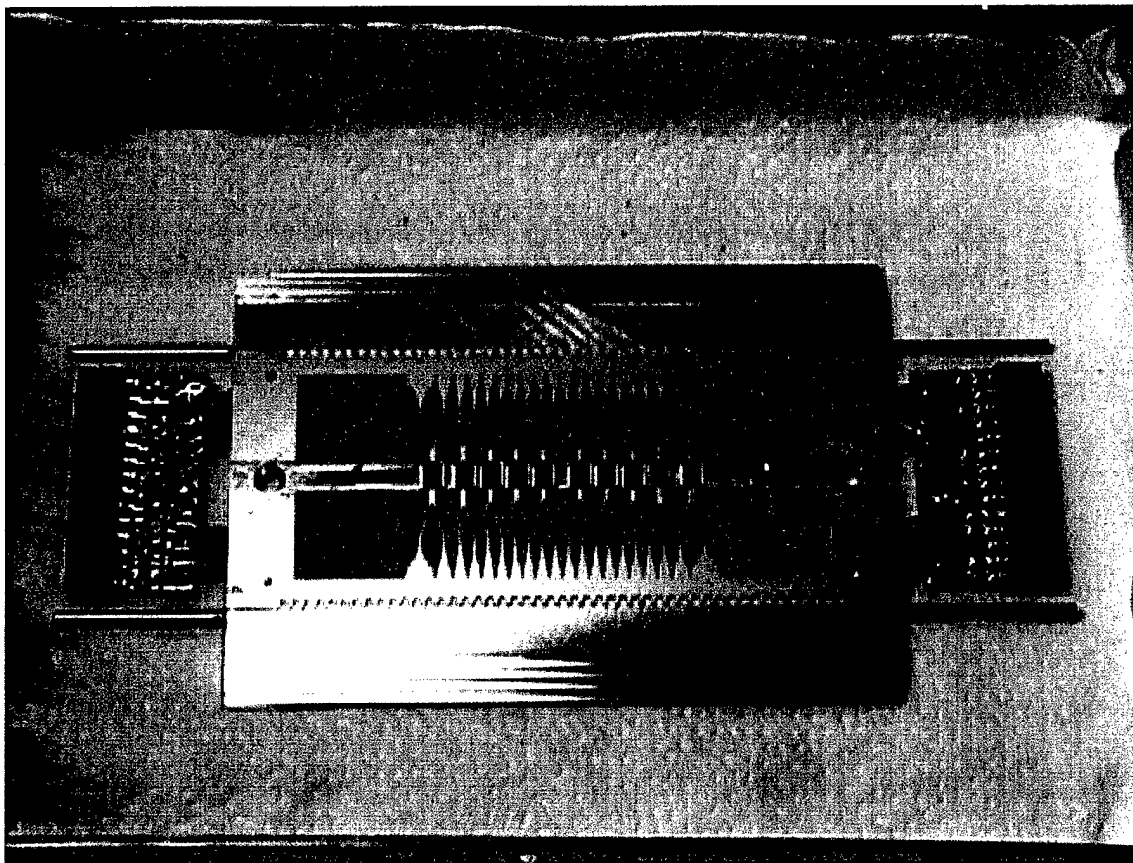
Figure 2.14: Single layer array amplifier with the RF boards and MMICs installed. Bias connectors and water-cooling pipes are visible on each side of the array.

The amplifiers were tested for oscillations at full dc power (V_{DD} = 5V, I_D = 500 mA) at frequencies ranging from 3 MHz to 60 GHz and found to be stable. Oscillations were only apparent at very high drain currents of 600 to 700 mA. Our previous experience with suppressing oscillations in these types of arrays is detailed in the previous Annual Report.

Small signal s-parameters were obtained at full dc power using an HP8510 with a 20 dB attenuator inserted in the output line. These results are shown in Fig. 15 where 20 dB should be added to the s_{21} scale. The amplifier shows a peak small signal gain of 15 dB and a typical gain of 10 dB over most of the upper half of Q-band. The nominal chip gain at full dc power is 17 dB. At reduced drain current of 250 mA the gain profile drops by 2 dB. The input reflection coefficient is typically –10 dB, rather than the typical –20 dB for the passive array and is due to the mediocre s_{11} of the chip (typically –8 dB). The output reflection coefficient, s_{22}, is off course dominated by the 20 dB attenuator.

A beam scan of the array amplifier output is shown in Figure 2.15. For this scan the output launcher section was removed so that the beam radiates from the stepped section of the array plates. The scan was obtained 10 mm from the stepped plate aperture.

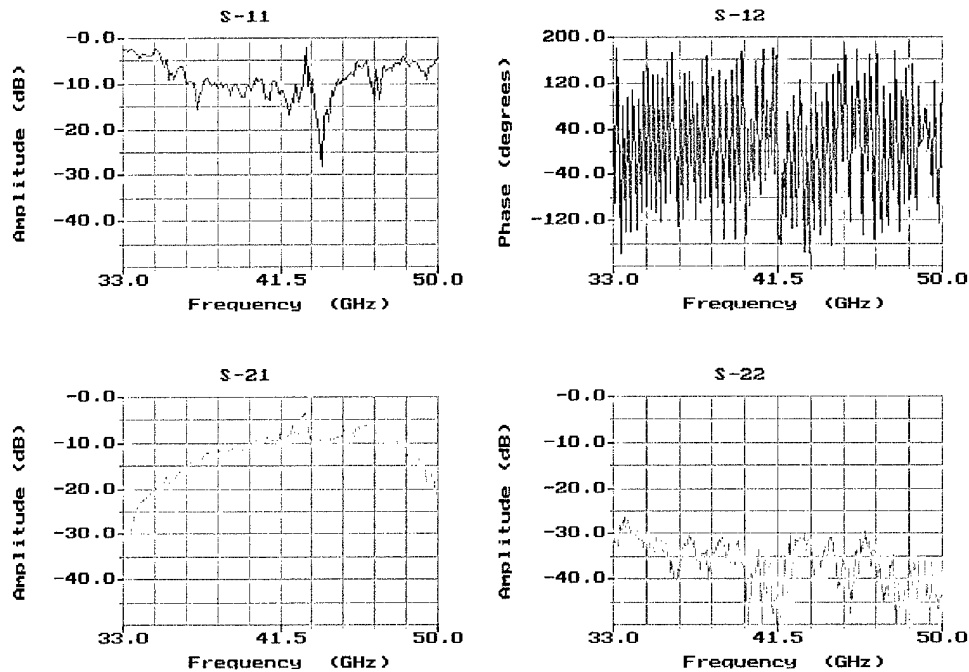**Figure 2.14: Single layer array amplifier small signal s-parameters at full dc power (V_{DD} = 5 V, I_D = 500 mA). The output is via a 20 dB attenuator so that 20 dB should be added to s₂₁.**
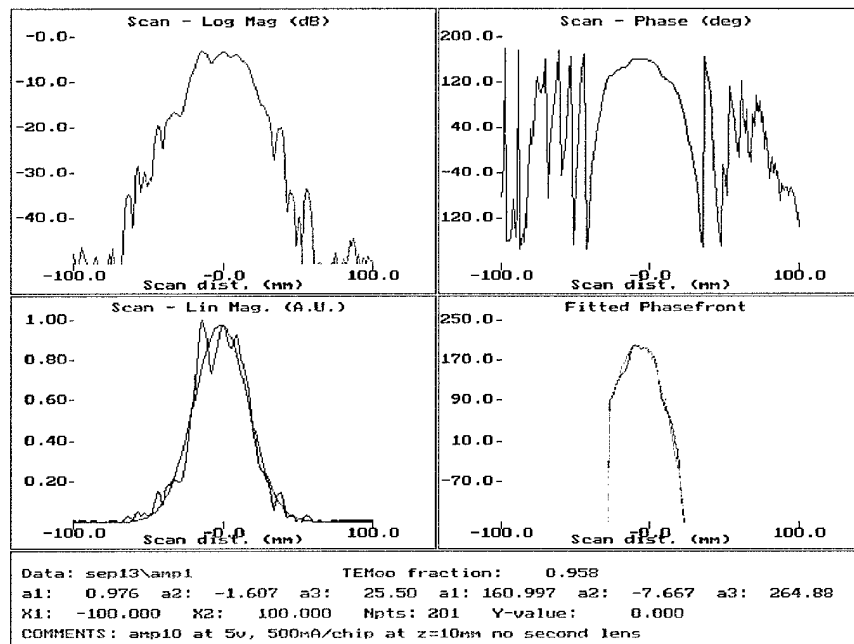

Figure 2.15: Beam scan of the output of the single layer array amplifier under small signal input and at full dc power.

The amplitude profile is still fairly square and the phase front shows the beam to be divergent as expected with a radius of curvature of 265 mm.

Power measurements were performed at 44 GHz using a 3.5 W Impatt oscillator as the input source. The input was supplied via a calibrated variable attenuator and a HP power meter was used to monitor the output power of the amplifier. The results at full dc power are shown in Figure 2.16. The power saturates at the −1 dB point at 27 dBm and the gain remains fairly constant in the large signal regime at 10.5 dB before falling at saturation.
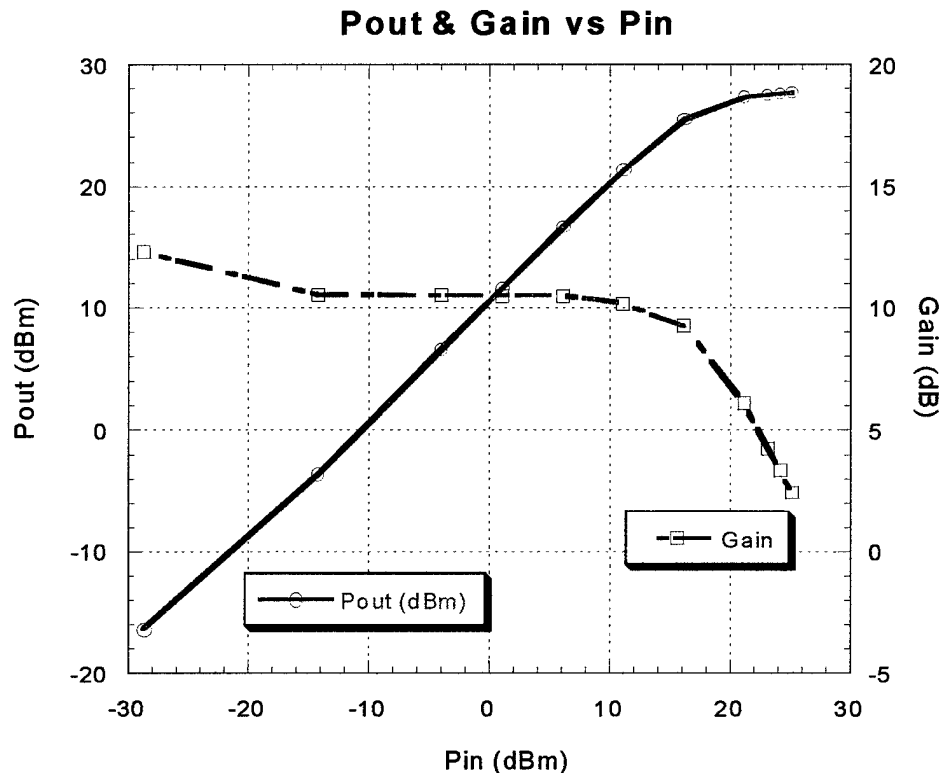
Pout & Gain vs Pin

Figure 2.16: Single layer array amplifier power measurements showing output power and gain as a function of input power up to full saturation.

With a nominal chip gain of 17 dB the 10.5 dB gain figure implies we have 6.5 dB of loss in the system. Our previous measurements on the passive single layer array showed a total insertion loss of 3 dB. Thus there is a shortfall of approximately 3.5 dB for the amplifier array. Beam scans comparing the radiated output of the amplifier array with the output of the passive array showed that, if anything, the amplifier array output was of better quality than the passive array output. The missing power was suspected to be the result of a poor interface between the chip and the 50Ω microstrip to which it was wire-bonded. In order to evaluate this hypothesis a MicroStripes simulation was performed on the chip-microstrip wire-bonded connection.
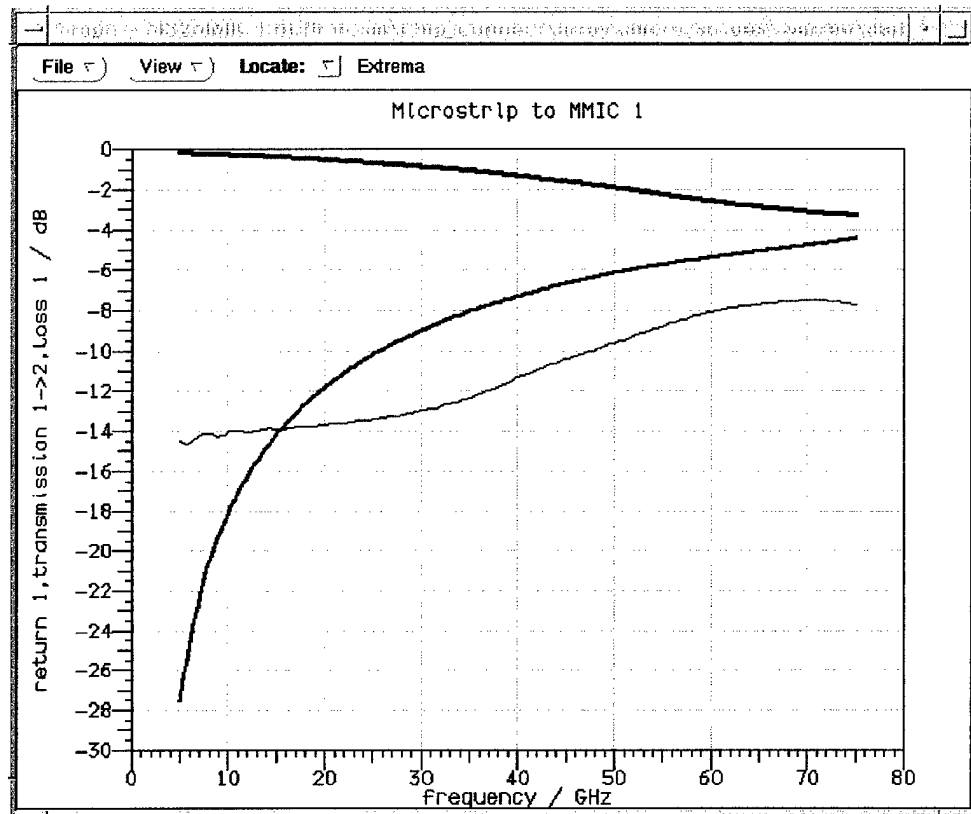
Figure 2.17: Microstrip to chip wire bond geometry. The chip substrate is 2 mil thick GaAs with a 50Ω line wire bonded to a 50Ω line on 15 mil thick TMM3.

The geometry of the simulation is shown in Fig. 17. The chip substrate is 2 mil thick GaAs with a 40 μm wide conductor (50Ω) and the TMM3 substrate is 15 mils thick with a 950 μm wide line. Dielectric and conductive losses are included. The s-parameter results in Fig. 18. At 44 GHz s_{21} is undergoing significant insertion loss – approximately 2 dB per bond wire connection. The reflection coefficient at −7dB is consistent with the small signal s-parameter measurements. The thin line shows the total losses $(1 - |s_{21}|^2 - |s_{11}|^2)$. These losses increase significantly above 30 GHz. Since the losses in this time domain based simulation are fixed for all frequencies (at the 44 GHz values) the increasing loss curve indicates that power is being radiated.

Figure 2.18: Microstrip to chip wire bond s-parameters from MicroStripes. Top line: s_{21}. Thin line: losses. Medium line: s_{11}.

In conclusion, the array amplifier architecture has been extensively investigated and is believed to be well understood. The packaging of the chip into its microstrip environment is responsible for approximately half of the insertion losses in this version of the array amplifier.

4.D Scientific Personnel (entire project)

Cornell University, SCREAM MEMS Group: Hercules Neves, Thomas Kudrle, Damien Rodger, Noel Elman.

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